The Neolithography Consortium

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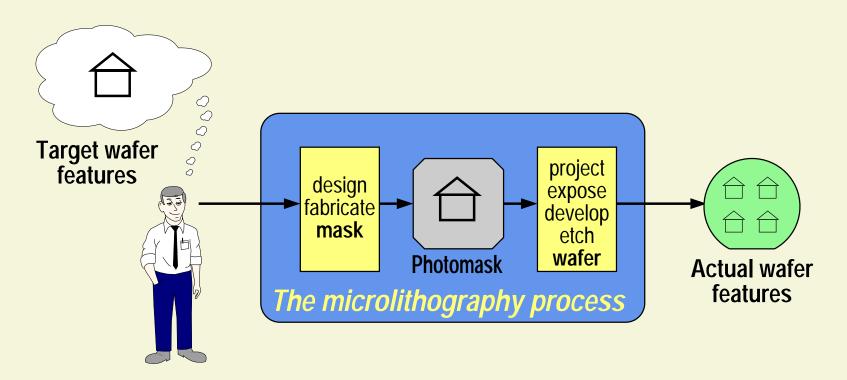
presented at the SPIE 25th International Symposium on Microlithography, paper 3998-54 (March, 2000).

Introduction

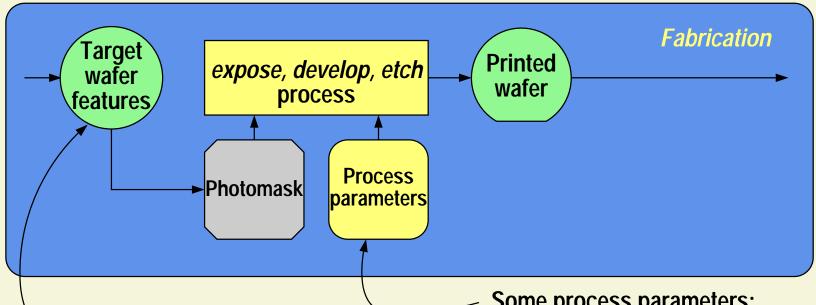
- wafer feature sizes are often smaller than the exposure wavelength
- nonlinearities inherent in the pattern transfer from photomask to wafer now become important
- note as evidence
 - the effectiveness of optical proximity correction (OPC)
 - the emerging importance of the mask error enhancement factor (MEEF)
- microlithography process simulation can accurately account for these now-important process nonlinearities
- however, the full benefit of simulation is not yet realized because of technical and economic factors

The goal of IC microlithography

Print the target wafer pattern with feature sizes and positions within their specified placement and CD tolerances



The microlithography process



Wafer pattern:

feature placements placement tolerances feature sizes size tolerances

Some process parameters:

exposure wavelength exposure NA coherence parameter illumination apodization wafer reflectivity resist thickness resist parameters exposure dose defocus

Process control

- Process control is needed for two reasons:
 - the process parameters are subject to variation
 - the process model is only approximate
- The paleolithographic model:

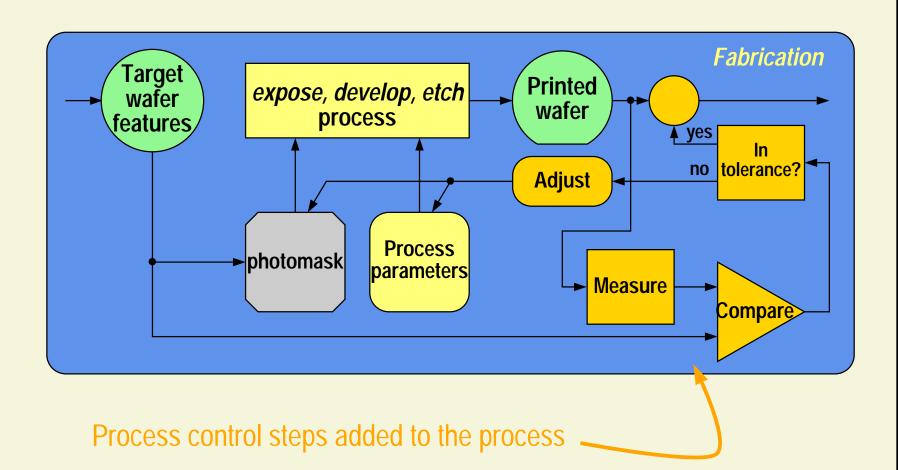
wafer pattern = mask pattern \times projection reduction ratio

- this approximation has served well for many years
- but now feature tolerances are on the same order as the nonlinear effects

Process parameter adjustment

- if the process nonlinearities are small, adjustments are small and approximately linear
- as nonlinearities become more important, adjustments become nonlinear and interdependent

Process control

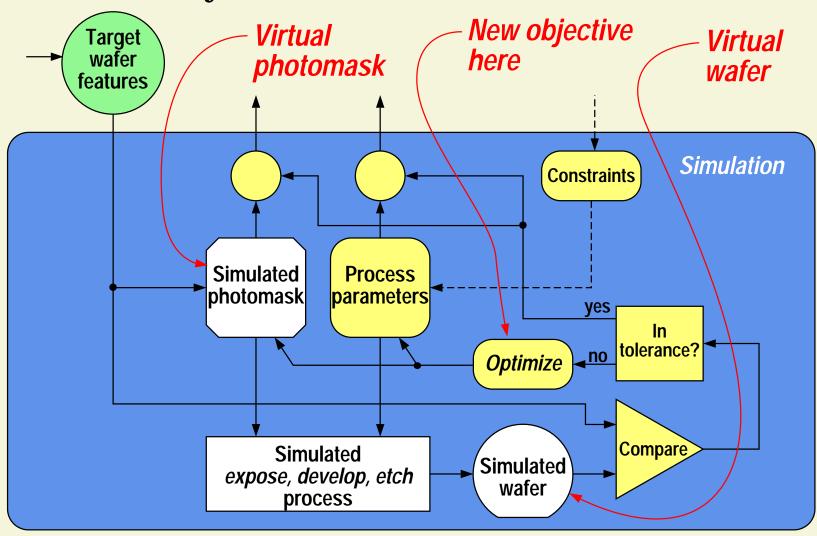


Neolithography

Neolithography *n* 1: a realistic photolithographic process in which the pattern on the photomask is not replicated exactly because of diffraction effects, subresolution mask features and imperfections, and other effects. 2: the design and control of such a process.

The neolithography process model-the "virtual fab"

Realized by means of simulation



The virtual fab

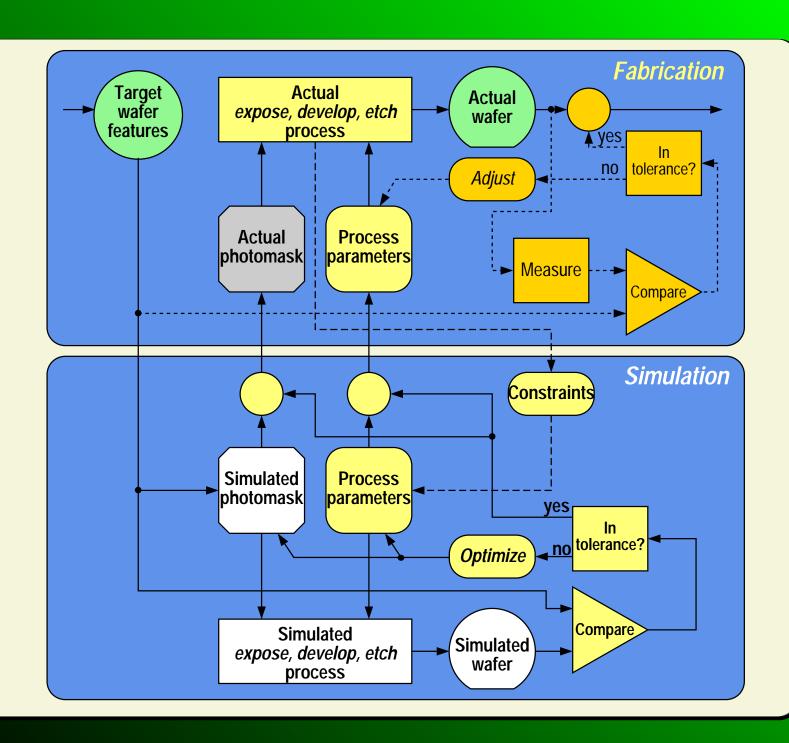
- entire simulation block is performed in software
 - prior to printing the first real wafer
 - one program comprised of snap-together applications
 - simulated objects are data files
- no measurements are required
- entire simulation and optimization can be automated
 - print as many virtual wafers as you like
- **operational description:**
 - enter wafer specifications
 - enter parameter constraints
 - enter parameter defaults
 - go to lunch

Simulation parameters subject to optimization or constraint

Table I Lithography simulation parameters

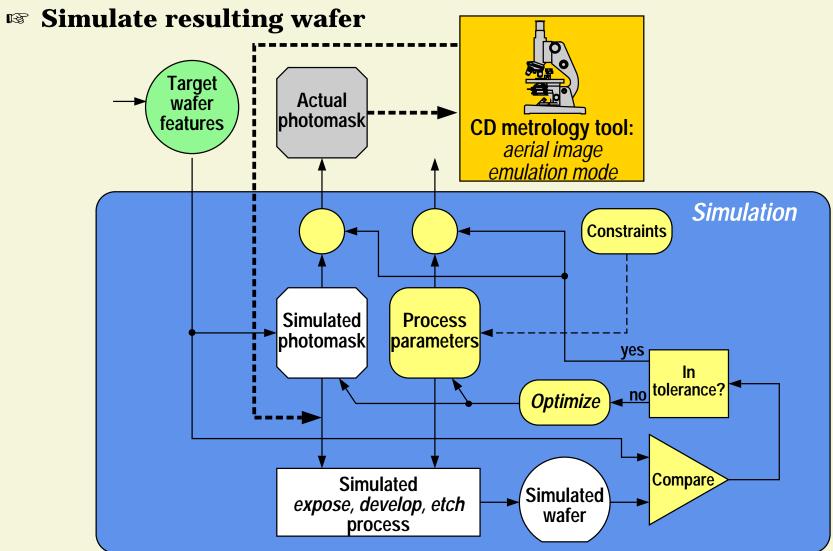
Photomask	lmage projection	Resist exposure	Etch		
specified mask chrome pattern and CDs specified mask phase shifters optical proximity corrections chrome thickness chrome edge shape chrome index of refraction	magnification exposure wavelength numerical aperture coherence parameter illumination geometry, apodization known projection lens aberrations and distortion wafer substrate reflectivity	resist thickness resist sensitivity resist index of refraction variation in index of refraction of exposed resist position of image focal plane in the resist (focus) exposure dose wafer substrate reflectivity resist development conditions post exposure bake	proximity effects etch parameters other stuff		

simulation Neolithography marries fabrication and

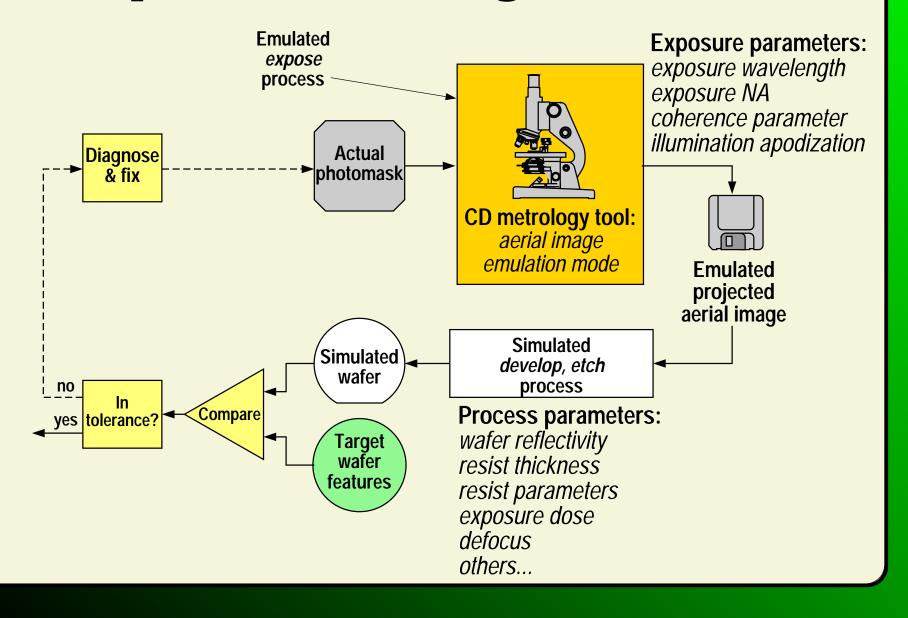


Photomask metrology

Emulate exposure aerial image from this actual mask



Exposure aerial image emulation



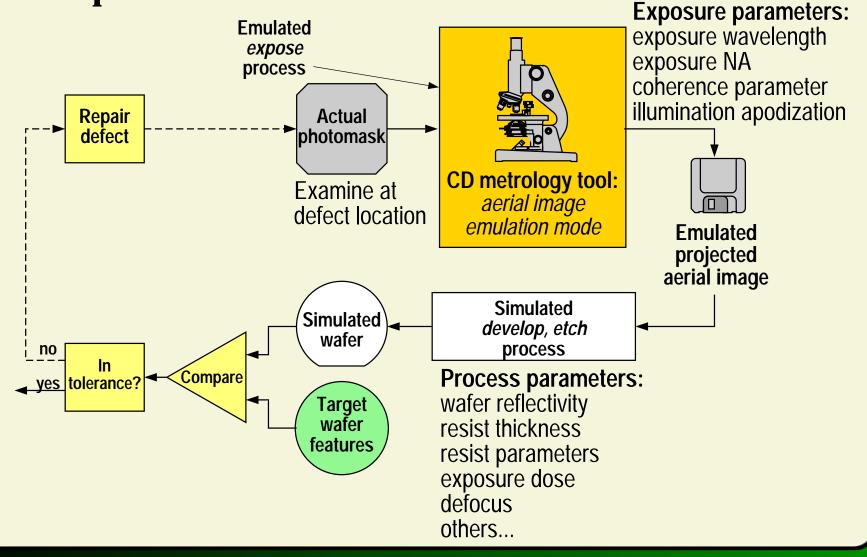
Mask parameters

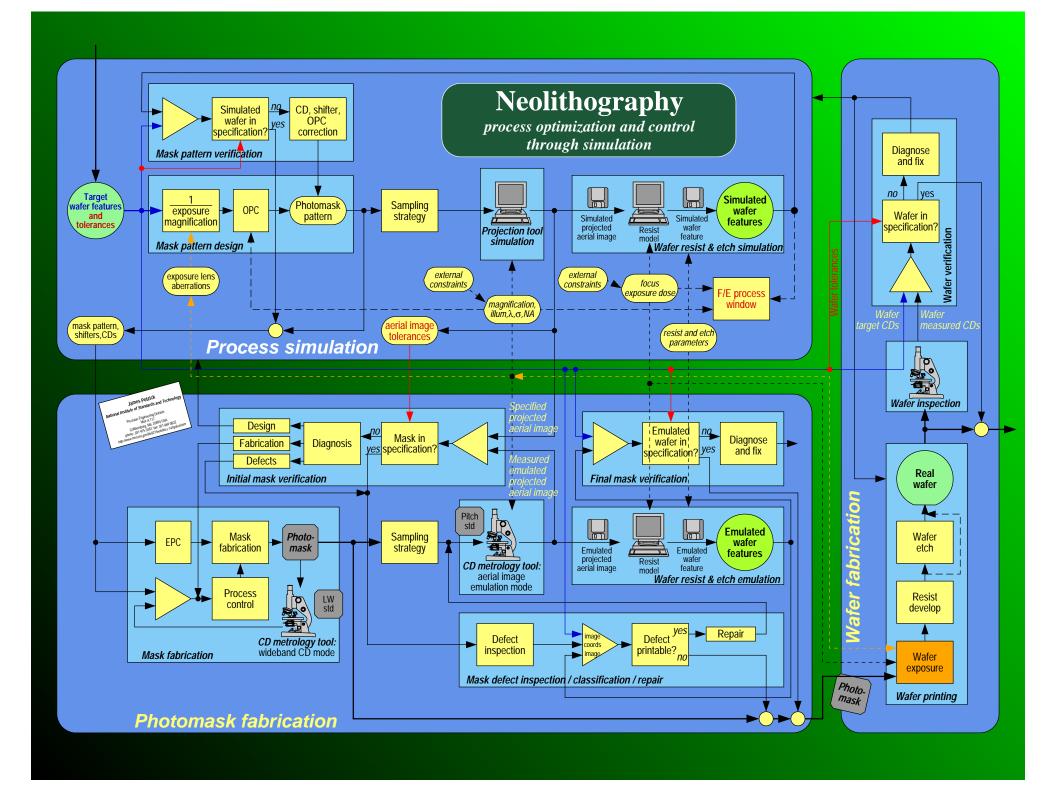
Table II Mask parameters uncovered in exposure emulation

Mask pattern errors	Chrome effects	Phase shifter errors	Mask substrate effects	Mask defects
feature placement errors OPC errors residual optical proximity effects mean-to- target errors across-plate variations plate-to-plate variations	edge runout edge roughness transmission at exposure wavelength phase shift at exposure wavelength other subresolution features and artifacts	dimensions placement phase shift at exposure wavelength image shift from phase errors	transmission at exposure wavelength substrate flatness mask support effects tilt of "plane of best focus" relative to substrate	defect printability defect proximity effects success of defect repair

Mask defect classification

Basically the same as mask metrology, but with emphasis on defect sites





In short...

Neolithography can *automatically optimize* the photomask design and the process parameters to *maximize the likelihood* that all wafer features *meet their CD and placement specifications*, before the first wafer is printed.

Benefits and costs of neolithography

Benefits

- automated photomask design based on wafer pattern specifications and process parameters
- automated optimization of photomask design and process parameters for robust process
- automated defect classification on the basis of printability
- accurate prediction of mask performance prior to exposing any wafers
- process can be re-optimized for specific measured photomask

Costs

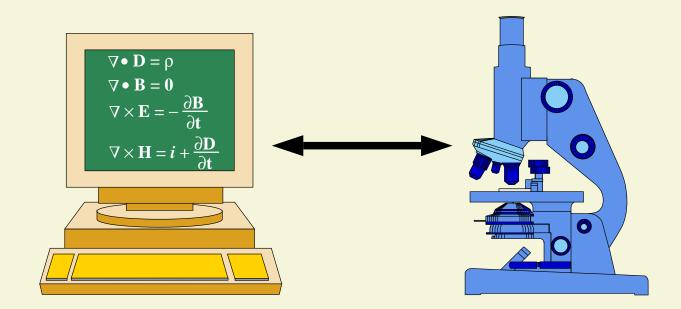
- capital cost of simulation tools
- design time consumed in simulations

The Consortium

- If neolithography is so wonderful, why is it not widely practiced?
 - not all simulation components are yet available
 - those that are available do not snap together
 - task is too large for any one company
 - processing time still long
- The Consortium is now being formed by NIST
 - a group of companies who develop or use simulation software
- **☞** its purpose
 - identify impediments to neolithography
 - remove them
 - for example
 - file format standards for data exchange
 - division of labor

Who should join the Consortium?

- suppliers and users of microlithography simulation or metrology tools
- **other interested parties**



Why join the Consortium?

Benefits to members

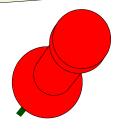
- members can influence standards development
- member's product is more valuable to customers
 - · easier to use
 - synergistic with other simulation applications
 - an essential part of an integrated simulation package
- common file formats, user interfaces, etc., reduce product design workload

Costs to members

- participation in 3 or 4 meetings per year
- homework
- underwriting of meeting logistics

Benefits to IC industry

- shorter design-to-product time
- lower production costs
- open standards encourage new software products



You are invited to an informal informational meeting for the NIST-sponsored

Neolithography Consortium

at SEMICON West time and place to be determined

James Potzick, NIST